A MECHANISM FOR SELF-INITIATED INSTRUCTION ISSUING AND METHOD THEREFOR

ABSTRACT OF THE DISCLOSURE

An apparatus and method for self-initiated instruction issuing are implemented. In a central processing unit (CPU) having a pipelined architecture, instructions are queued for issuing to the execution unit which will execute them. Instructions are issued each cycle, and an instruction should be selectable for issuing as soon as its source operands are available. An instruction in the issue queue having source operands depending on other, target, instructions to determine their value are signaled to the target instruction by a link mask in the queue entry corresponding to the target instruction. A bit in the link mask identifies the queue entry corresponding to the dependent instruction. When the target instruction issues to the execution unit, a bit is set in a predetermined portion of the queue entry containing the dependent instruction. The portion of the queue entry is associated with the source operand depending on the issuing instruction. This bit informs selection logic circuitry that the dependency is resolved by the issuing instruction, and the dependent instruction may be selected for issuing.